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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/611,955	07/06/2000	Cyprian Emeka Uzoh	FIS919970205US2	6678

32074 7590 04/08/2008

INTERNATIONAL BUSINESS MACHINES CORPORATION
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BLDG. 300-482
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EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

MAIL DATE	DELIVERY MODE
04/08/2008	PAPER

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CYPRIAN EMEKA UZOH and
STEPHEN EDWARD GRECO

Appeal 2008-0277
Application 09/611,955
Technology Center 2800

Decided: April 8, 2008

Before CHARLES F. WARREN, LINDA M. GAUDETTE, and
MICHAEL P. COLAIANNI, *Administrative Patent Judges*.

COLAIANNI, *Administrative Patent Judge*.

DECISION ON APPEAL

1Appellants appeal under 35 U.S.C. § 134 the final rejection of claims 25-32. We have jurisdiction over the appeal pursuant to 35 U.S.C. § 6(b).

We REVERSE.

INTRODUCTION

Appellants claim a semiconductor structure comprising, in relevant part, a semiconductor substrate with a recess located in at least one major surface of said semiconductor substrate having a conductive metal in the

recess only (claim 25). Appellants disclose that the metal deposited in the recess functions as multilevel wiring for chip interconnections (Spec. 1).

Claim 25 is illustrative:

25. A semiconductor structure, comprising: a semiconductor substrate; a recess located in at least one major surface of said semiconductor substrate; an electrical insulating layer located over said at least one major surface and in said recess; a conductive barrier located over said insulating layer in said recess and over said at least one major surface; a plating seed layer located over said conductive barrier within said recess only; and a conductive metal in said recess only.

The Examiner relies on the following prior art references as evidence of unpatentability:

Shibata	4,577,395	Mar. 25, 1986
Jain	5,821,168	Oct. 13, 1998
Maekawa	6,329,284 B2	Dec. 11, 2001

The rejections as presented by the Examiner are as follows:

1. Claims 25 and 28-32 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jain in view of Shibata.
2. Claims 26 and 27 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Jain in view of Shibata and Maekawa.

The Examiner finds that Jain discloses all of the features of claim 25, except that Jain's semiconductor structure (i.e., an interconnect structure 74) is not formed in a semiconductor substrate (Ans. 4). The Examiner finds that Shibata discloses forming a semiconductor structure (i.e., a memory device) in a semiconductor substrate (Ans. 4). Based on these teachings, the Examiner concludes that it would have been obvious to form the semiconductor device (i.e., the interconnect structure 74) of Jain in the

semiconductor substrate, such as taught by Shibata, in order to increase the packing density with the formation of a plurality of structures (Ans. 4).

OPINION

Appellants argue that Shibata is not properly combinable with Jain (Br. 6). Appellants contend that modifying Jain's structure to place interconnects in the semiconductor substrate would be contrary to Jain's objectives of providing an inlaid structure 74 (i.e., interconnects) for connection with the lower interconnects 28 (Br. 6).

We agree with Appellants' arguments and, therefore, cannot sustain the Examiner's § 103 rejections for the reasons below.

The Examiner bears the initial burden of establishing a prima facie case. *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). Hindsight must not be used in the selection of references that comprise the case of obviousness. *In re Rouffet*, 149 F.3d 1350, 1358 (Fed. Cir. 1998). If examination at the initial stage does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of the patent. *Oetiker*, 977 F.2d at 1445.

Jain discloses processes for forming inlaid interconnects (Jain, col. 1, ll. 6-9). Jain discloses that dual inlaid structures 74 (i.e., interconnects) are formed in a second insulating layer 52 (Jain, col. 4, ll. 33-41; Figure 9). Jain further discloses that the process may be used to form interconnects in layers overlying the inlaid structures 74 (i.e., interconnects) or in the upper insulating layer 30 located below the insulating layer 52 (Jain, col. 4, ll. 46-55). Jain does not disclose forming the inlaid structures (i.e., interconnects) in the semiconductor substrate.

Shibata discloses a method of forming a trench memory capacitor on a semiconductor substrate (Shibata, col. 1, ll. 8-12). Shibata discloses that forming a groove or trench in a semiconductor substrate permits the capacitor to be more highly integrated on the surface of the semiconductor (Shibata, col. 1, ll. 9-11). Shibata discloses that the grooves permit the surface area of the capacitor to be increased thereby increasing the capacitance of the device, while shrinking the area occupied by the capacitor on the semiconductor surface (Shibata, col. 1, ll. 12-32).

Based on these disclosures, the Examiner improperly concludes that it would have been obvious to modify Jain's interconnect structure such that the interconnect structure is formed in the semiconductor substrate because Shibata discloses that forming the grooves into the semiconductor substrate permits a high integration of a semiconductor structure (i.e., the memory capacitor) on the substrate (Ans. 4 and 7).

Jain's invention is directed to forming an interconnect structure on a semiconductor device. Shibata is directed to forming a memory capacitor in a semiconductor substrate. Shibata forms the grooves or trenches in the semiconductor substrate to permit the capacitor to be highly integrated without the loss in capacitance associated with decreasing the size of the capacitor. In other words, the grooves or trenches permit the surface area of the capacitor to be increased, while also decreasing the size the capacitor occupies on the semiconductor substrate.

In light of these disclosures, Shibata's use of grooves to permit a capacitor to be highly integrated on a semiconductor substrate without reduction in capacitance would not have suggested to one of ordinary skill in the art that Jain's interconnects may be highly integrated on a semiconductor

substrate by using grooves as the Examiner determines. The Examiner has improperly used hindsight in determining that Shibata's disclosures regarding grooves or trenches with capacitors would have suggested forming Jain's interconnects in a semiconductor substrate. *Rouffet*, 149 F.3d at 1358.

Because no prima facie case of obviousness has been established by the Examiner, we cannot sustain the Examiner's § 103 rejection of claims 25 and 28-32 over Jain in view of Shibata, or the § 103 rejection of dependent claims 26 and 27 over Jain in view of Shibata and Maekawa.

DECISION

The Examiner's decision is reversed.

REVERSED

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